PSG5400
DATA SHEET
Preliminary

Switching Regulator Supervisor with On-Demand Power® for DDR Memory VDDQ

Features

- Configurable On-Demand Power® algorithm to adaptively scale regulator output voltage in correlation with monitored activity
- Sensory interface to monitor activity and demand for the controlled voltage domain
- Programmable output voltage supporting DDR3, DDR3L, DDR3UL, and DDR4
- Serial programming interface
- QFN package

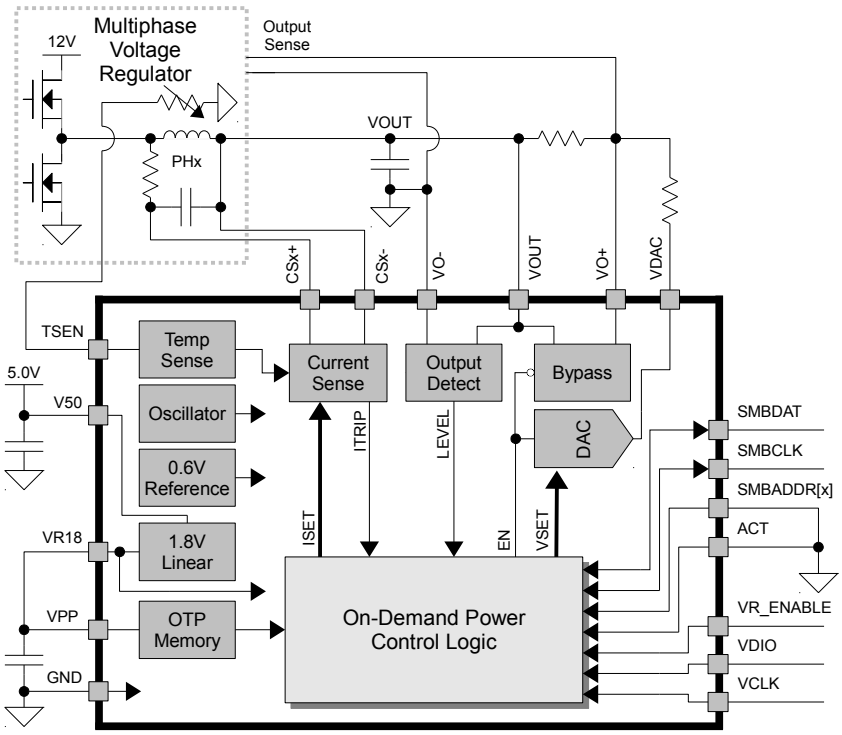
Description

The PSG5400 is a highly integrated power management IC with a differential remote sense voltage regulator interface designed to monitor DDR memory activity and scale the VDDQ supply voltage dynamically. A programmable interface for monitoring memory activity, coupled with an advanced On-Demand Power® algorithm, enable the supply voltage of the memory voltage regulator to be adaptively scaled in correlation with actual demand. The real-time tracking of supply voltage to memory activity enables maximum system power savings by minimizing the power spent on maintaining worst-case headroom in the power distribution network.

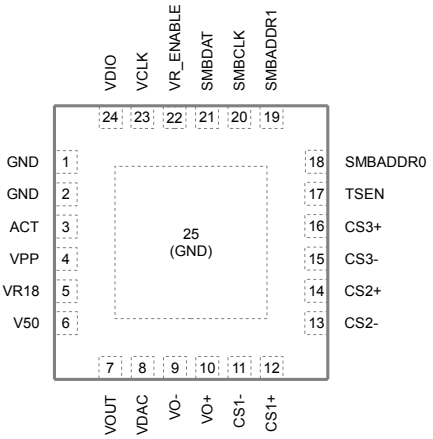
Applications

- DDR3, DDR3L, DDR3UL, DDR4 Memory Power Supplies
- Mobile computers
- Servers
- Network switches and routers

Functional Diagram



QFN Package



24-LEAD (5mm x 5mm) PLASTIC QFN
EXPOSED PAD (PIN 25) IS GROUND CONNECTION.
MUST BE SOLDERED TO PCB.

Absolute Maximum Ratings (Note 1)

PARAMETER	VALUE	UNIT
V50 to GND	-0.3 to 6	V
VR18, VDIO, VCLK to GND	-0.3 to 2.0	V
VO+, VO-, CSx+, and CSx- to GND	-0.3 to 6	V
CSx+ and CSx- to V50	0.3	V
All other pins to GND	-0.3 to 6.0	V
All other pins to V50	0.3	V
Maximum Junction Temperature	125	°C

Note 1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Electrical Characteristics

Unless otherwise noted: V_{V50} = 5V, V_{V18} = 1.8V, V_{GND} = 0V, V_{VR_ENABLE} = V_{SMBDAT} = V_{SMBCLK} = V_{ACT} = 3.3V, VR18 = No external load, T_A = 0°C to 85°C (Note 2). Typical values are at T_A = 25°C.

PRELIMINARY INFORMATION

Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{V18}	Digital and analog supply voltage		1.62	1.8	1.98	V
V_{V50}	Analog supply voltage		4.5	5	5.5	V
T_A	Operating ambient temperature		0		85	°C

Power Supplies

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{V18}	Digital and analog supply current Enabled Disabled	 V_{VR_ENABLE} = 3.3V V_{VR_ENABLE} = 0V			 1.7 28	 mA µA
I_{V50}	Analog supply current Enabled Disabled	No load on VR18 output V_{VR_ENABLE} = 3.3V V_{VR_ENABLE} = 0V			 1.6 48	 mA µA

Two-Wire Interface

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus clock frequency		10		100	kHz
$t_{TIMEOUT}$	SMBDAT and SMBCLK time low for reset of SMBus	(Note 3)	25		35	ms

1MHz Oscillator

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{1MHZ}	Internal oscillator frequency		0.9		1.1	MHz

Thermistor Interface (TSEN)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
R_{25}	Thermistor nominal resistance	25°C	45.6	47.0	48.4	kΩ
$\beta_{25/100}$	Thermistor β coefficient			4,000		

Digital Interface

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SMBDAT, SMBCLK Inputs						
V_{IH}	Input high voltage				2.1	V
V_{IL}	Input low voltage		0.8			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 5V			5	µA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			-5	µA
ACT Input						
V_{IH}	Input high voltage	ACT Low Voltage Input = 0 ACT Low Voltage Input = 1			1.4 0.65	V
V_{IL}	Input low voltage	ACT Low Voltage Input = 0 ACT Low Voltage Input = 1	0.8 0.35			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 5V			10	µA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			-10	µA
VR_ENABLE						
V_{IH}	Input high voltage				1.31	V
V_{IL}	Input low voltage		0.81			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 3.3V			5	µA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			-5	µA
VCLK, VDIO						
V_{IH}	Input high voltage				0.88	V
V_{IL}	Input low voltage		0.53			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 1.05V			10	µA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			-10	µA
SMBDAT Output						
V_{OL}	Low level output voltage	I_{OL} = 2mA			0.4	V
I_{OH}	High level output leakage current	Output Voltage = 5V			5	µA

1.8V Linear Regulator

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{VR18}	1.8V linear regulator output voltage	$0 < I_{VR18} < 5mA$	1.71		1.98	V

Current Sense

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_p	Propagation delay	$\sum(V_{CSx+} - V_{CSx-})$ = 2mV to 60mV, ITRIP = 31mV		10		µs
I_{CSx}	CS± input bias current	$V_{CSx±}$ = 0.80V to 1.52V			120	nA
$V_{TRIP(60)}$	Programmable trip voltage	ISETx[7:0] = TBD		60		mV
$V_{TRIP(2)}$	Programmable trip voltage	ISETx[7:0] = TBD		2		mV

Note 2 Parts are tested at 25°C and 85°C. Temperature limits established by characterization and are not production tested.
Note 3 Exceeding $t_{TIMEOUT}$ will reset the SMBus state machine, therefore setting SMBDAT and SMBCLK pins to a high impedance state.

Pin Functions

NAME	PIN	IO (Note 4)	DESCRIPTION
V50	6	P	5V power supply for analog circuitry. Decouple each pin to GND with a capacitor
GND	1, 2, 25	P	Small signal ground. All small signal components should connect to this ground. Pin 25 is the exposed pad
VPP	4	P	One Time Programmable (OTP) programming voltage. This should be connected to VR18 during normal operation.
VR18	5	A	Internal 1.8V linear regulator output. Decouple to GND with a capacitor
CSx+	12, 14, 16	A	Current sense differential amplifier input. The positive input to the amplifier is normally connected to current sensing resistors through an RC filter
CSx-	11, 13, 15	A	Current sense differential amplifier input. The negative input to the amplifier is normally connected to current sensing resistors through an RC filter
TSEN	17	A	Temperature Sense Input
VDAC	8	A	DAC output voltage
VOUT	7	A	Voltage regulator output voltage
VO+	10	A	Voltage regulator output voltage remote sense input
VO-	9	A	Voltage regulator output voltage remote sense input
ACT	3	I	Activity input. Logic threshold level is digitally programmable. A logic low indicates that the respective load is active. A logic high indicates that the respective load is idle. Do not leave floating.
SMBDAT	21	IOD	SMBus data input/output. The PSG5400 is configured as an SMBus device.
SMBCLK	20	IOD	SMBus clock input. The PSG5400 is configured as an SMBus device.
SMBADDRx	18, 19	I	SMBus address input. This configures the PSG5400 device to one of four different SMBus addresses
VCLK	23	I	SVID Clock
VDIO	24	I	SVID Data
VR_ENABLE	22	I	Enable input. A logic low forces the PSG5400 into a low-power standby mode. A logic high enables the PSG5400. Connect directly to V50 if not used. Do not leave this pin floating.

Note 4 P = Power, A = Analog, I = Input, O = Output, OD = Open Drain, IOD = Bidirectional Open Drain, X = Unconnected

1 Two Wire Interface

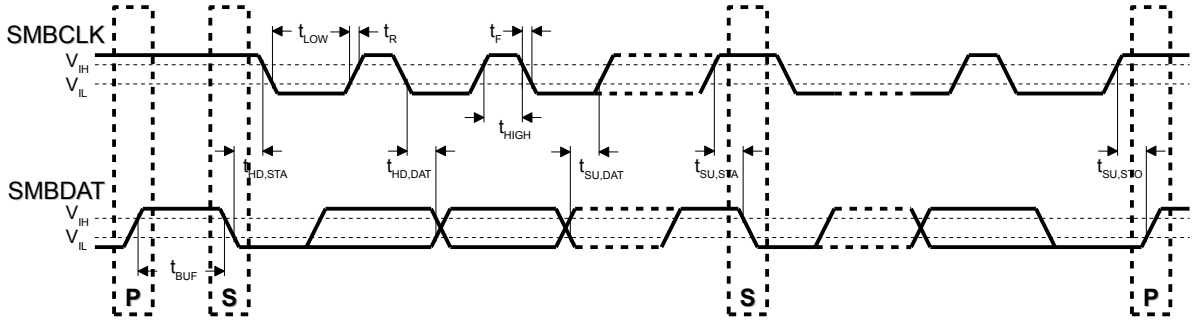
The PSG5400 serial interface is compatible with the SMBus 2.0 specification. SMBCLK is the serial clock input and SMBDAT is the bidirectional serial data. PSG5400 supports 'read byte', 'write byte', and 'block write' as described by the SMBus specification.

1.1 Serial Address

PSG5400 is configured as a slave and has a fixed 7-bit slave address of 11000XX (0x60 – 0x63), configurable through digital input pins SMBADDR0 and SMBADDR1. Tie each SMBADDRx pin to GND for logic 0 and 5V for logic 1. The following table outlines SMBADDR0/SMBADDR1 pin operation:

SMADDR1	SMADDR0	Serial Address
0	0	0x60
0	1	0x61
1	0	0x62
1	1	0x63

1.2 Timing Diagram



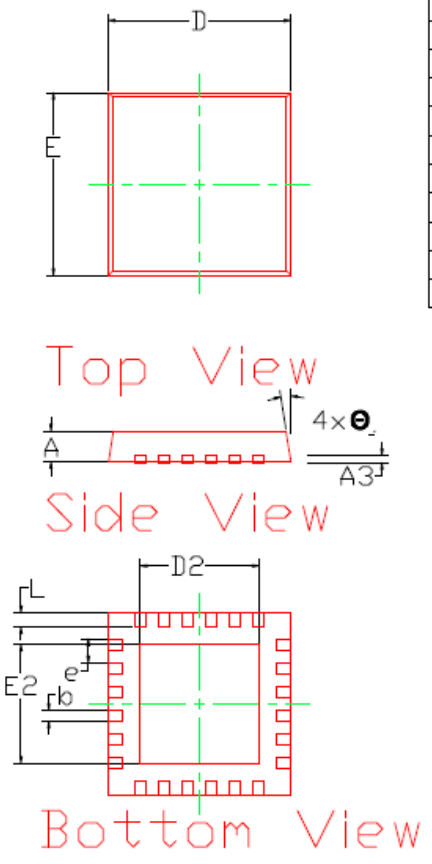
1.3 Address Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	NAME	DEFAULT VALUE
00H-11H	Reserved								RESERVED	
12H	Reserved	ODP_STATE			Reserved	VOUT_DET	BYPASS1	ODP_EN	ODPCON	0x02
13H	ODP Static High Output Voltage								ODPVOUT0_HIGH	0x00
14H	ODP State 1 High Output Voltage								ODPVOUT1_HIGH	0x00
15H	ODP State 2 High Output Voltage								ODPVOUT2_HIGH	0x00
16H	ODP State 3 High Output Voltage								ODPVOUT3_HIGH	0x00
17H	ODP State 4 High Output Voltage								ODPVOUT4_HIGH	0x00
18H	ODP State 1 High Current Threshold								ODPITH1_HIGH	0x00
19H	ODP State 2 High Current Threshold								ODPITH2_HIGH	0x00
1AH	ODP State 3 High Current Threshold								ODPITH3_HIGH	0x00
1BH	ODP Static Low Output Voltage								ODPVOUT0_LOW	0x00
1CH	ODP State 1 Low Output Voltage								ODPVOUT1_LOW	0x00
1DH	ODP State 2 Low Output Voltage								ODPVOUT2_LOW	0x00
1EH	ODP State 3 Low Output Voltage								ODPVOUT3_LOW	0x00
1FH	ODP State 4 Low Output Voltage								ODPVOUT4_LOW	0x00
20H	ODP State 1 Low Current Threshold								ODPITH1_LOW	0x00
21H	ODP State 2 Low Current Threshold								ODPITH2_LOW	0x00
22H	ODP State 3 Low Current Threshold								ODPITH3_LOW	0x00
23H	Reserved	VOUT Threshold 1			Reserved	VOUT Threshold 0			VOUT_TH0	0x00
24H	Reserved	VOUT Threshold 3			Reserved	VOUT Threshold 2			VOUT_TH1	0x00
25H	Reserved					VOUT Threshold 4			VOUT_TH2	0x00
26H	ODP Timeout 0 [7:0]								ODPTOUT0_0	0x00
27H	ODP Timeout 0 [15:8]								ODPTOUT0_1	0x00
28H	ODP Timeout 0 [23:16]								ODPTOUT0_2	0x00
29H	ODP Timeout 1 [7:0]								ODPTOUT1_0	0x00
2AH	ODP Timeout 1 [15:8]								ODPTOUT1_1	0x00
2BH	ODP Timeout 1 [23:16]								ODPTOUT1_2	0x00
2CH	ODP Timeout 2 [7:0]								ODPTOUT2_0	0x00
2DH	ODP Timeout 2 [15:8]								ODPTOUT2_1	0x00
2EH	ODP Timeout 2 [23:16]								ODPTOUT2_2	0x00
2FH	ODP Timeout 3 [7:0]								ODPTOUT3_0	0x00
30H	ODP Timeout 3 [15:8]								ODPTOUT3_1	0x00
31H	ODP Timeout 3 [23:16]								ODPTOUT3_2	0x00
32H	Prescale	ODP Rising Slew Rate 0							ODPSLEWUP0	0x00
33H	Prescale	ODP Rising Slew Rate 1							ODPSLEWUP1	0x00

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	NAME	DEFAULT VALUE
34H	Prescale	ODP Rising Slew Rate 2							ODPSLEWUP2	0x00
35H	Prescale	ODP Rising Slew Rate 3							ODPSLEWUP3	0x00
36H	Prescale	ODP Falling Slew Rate 1							ODPSLEWDOWN1	0x00
37H	Prescale	ODP Falling Slew Rate 2							ODPSLEWDOWN2	0x00
38H	Prescale	ODP Falling Slew Rate 3							ODPSLEWDOWN3	0x00
39H	Prescale	ODP Falling Slew Rate 4							ODPSLEWDOWN4	0x00
3AH	VOUT Detect Blanking Time								VOUTBLANK	0x00
3BH	ODP Activity Configuration								ODPACT	0x00
3CH	SVID Monitor Configuration								SVID_CONF	0x00
3DH	Reserved								RESERVED	
3EH	ODP Slew Up to S2 Step Count				ODP Slew Up to S1 Step Count				ODPSLEWUPCNT0	0x00
3FH	ODP Slew Up to S3 Step Count				ODP Slew Up to S4 Step Count				ODPSLEWUPCNT1	0x00
40H	ODP Slew Down to S1 Step Count				ODP Slew Down to S0 Step Count				ODPSLEWDNCNT0	0x00
41H	ODP Slew Down to S3 Step Count				ODP Slew Down to S2 Step Count				ODPSLEWDNCNT1	0x00
42H-FFH	Reserved								RESERVED	

Packaging

The PSG5400 is packaged in a 5mmX5mm 24-pin QFN. All dimensions are in millimeters unless otherwise noted.



DIMENSION (mm)				
SYMBOL	MIN	NOM	MAX	TOL.
A		0.850		+/- 0.1
A3		0.203		
b	0.250	0.300	0.350	
D		5.000		
D2	3.150	3.250	3.350	
E		5.000		
E2	3.150	3.250	3.350	
e		0.650		
L	0.350	0.400	0.450	
Θ	0 deg.		14 deg.	