PSG2410

DATA SHEET
Preliminary

Low Dropout Regulator with On-Demand Power® for DDR Memory VDDQ

Features

- Configurable On-Demand Power® algorithm to adaptively scale regulated output voltage in correlation with monitored activity
- Sensory interface to monitor activity and demand for regulated voltage domain
- Ultra-low dropout voltage regulator architecture
- Input voltage range: 1.15V to 1.6V
- 3.5A output current
- High efficiency bypass mode
- Programmable output voltage supporting DDR3, DDR3L, DDR3UL, and LPDDR2
- Serial programming interface
- QFN package

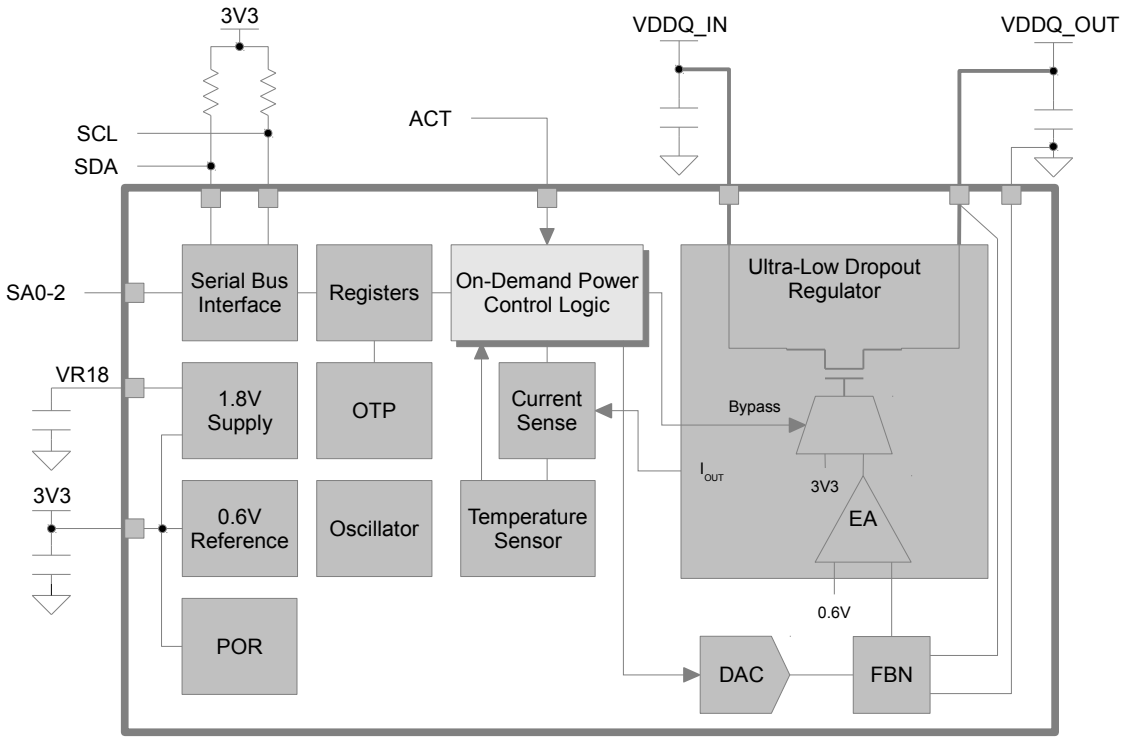
Description

The PSG2410 is a highly integrated power management IC with an ultra-low dropout voltage regulator designed to supply VDDQ to DDR memory. A programmable interface for monitoring memory activity, coupled with an advanced On-Demand Power® algorithm, enable the regulated output voltage of the integrated regulator to be adaptively scaled in correlation with actual demand. The real-time tracking of supply voltage to memory activity enables maximum system power savings by minimizing the power spent on maintaining worst-case headroom in the power distribution network.

Applications

- LPDDR2 Memory Power Supplies
- DDR3, DDR3L, DDR3UL Memory Power Supplies
- Mobile computers
- Servers
- Network switches and routers

Functional Diagram



Absolute Maximum Ratings (Note 1)

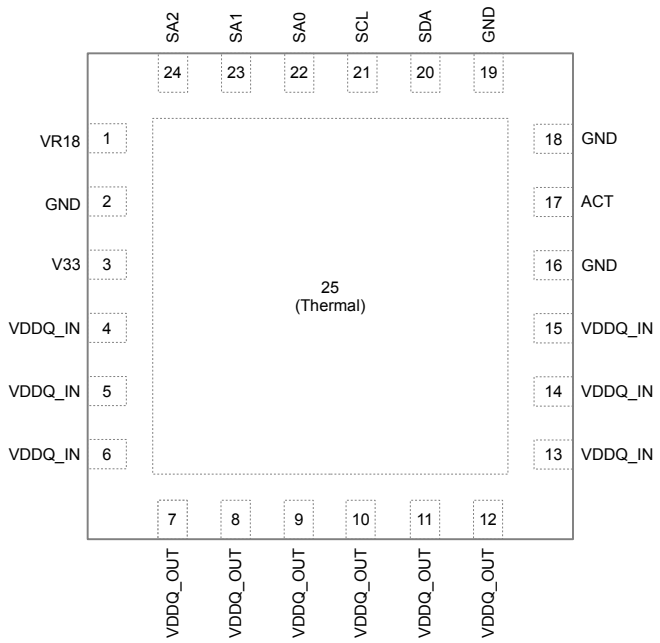
PARAMETER	VALUE	UNIT
VDDQ_IN to GND	-0.3 to 2.0	V
V33 to GND	-0.3 to 3.6	V
All other pins to GND (Note 2)	-0.3 to 3.6	V
All other pins to V33 (Note 3)	0.3	V
Maximum Junction Temperature	125	°C

Note 1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2 Pin SA0 does not support the V_{HV} levels used in the Serial Presence Detect Set, Clear, and Read Software Write Protection commands. Add a series resistor and a suitable voltage clamping device if these commands are to be used with the PSG2410 connected to the same SA0 as the SPD device.

Note 3 SMBus pins SA0, SA1, SA2, SCL, and SDA are excluded from this.

PINOUT



24-LEAD (5mm x 5mm) PLASTIC QFN
EXPOSED PAD (PIN 25) IS THERMAL CONNECTION, MUST BE SOLDERED TO PCB.

Electrical Characteristics

Unless otherwise noted: VDDQ_IN = 1.35V, V33 = SDA = SCL = ACT = 3.3V, GND = 0V, VR18 = No external load, T_A = 0°C to 95°C (Note 4). Typical values are at T_A = 25°C.

PRELIMINARY INFORMATION

Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VDDQ_IN	Input Voltage		1.15		1.6	V
V_{V33}	Bias supply voltage		3.0	3.3	3.6	V
T_A	Operating ambient temperature		0		95	°C

Power Supplies

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{V33}	Bias supply current	ODP Enabled (ODP_EN = 1) ODP Disabled (ODP_EN = 0)			10 1	mA mA
I_{VDDQ_IN}	Linear regulator supply current	No Load on VDDQ_OUT				µA

Digital Interface

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SDA, SCL Inputs						
V_{IH}	Input high voltage				2.1	V
V_{IL}	Input low voltage		0.8			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 3.3V			5	µA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			-5	µA
ACT Input						
V_{IH}	Input high voltage				1.4	V
V_{IL}	Input low voltage		0.8			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 3.3V			10	µA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			-10	µA
SDA Output						
V_{OL}	Low level output voltage	I_{OL} = 2mA			0.4	V
I_{OH}	High level output leakage current	Output Voltage = 3.3V			5	µA

Two-Wire Interface

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus clock frequency		10		400	kHz
$t_{TIMEOUT}$	SDA and SCL time low for SMBus reset	(Note 5)	25		35	ms

4MHz Oscillator

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{4MHZ}	Internal oscillator frequency		3.6	4.0	4.4	MHz

Ultra-Low Dropout Linear Regulator

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DROPOUT}$	Dropout Voltage	I_{LOAD} = 3A, V33 - V_{DDQ_IN} ≥ 1.80V I_{LOAD} = 3A, V33 - V_{DDQ_IN} ≥ 1.62V			50 75	mV
I_{OCP}	Current Limit			3500		mA
	Line Regulation				2	%
	Load Regulation				2	%
	Phase Margin	C_{OUT} = 100µF ceramic		60		°
Bypass Switch						
R_{ON}	On-Resistance			17		mΩ

1.8V Linear Regulator

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{VR18}	1.8V linear regulator output voltage	0 < I_{VR18} < 5mA	1.71		1.98	V

Current Sense

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_p	Propagation delay			4		µs
$I_{TRIP(D4)}$	Programmable trip current	ISETx[7:0] = 0xB6		2500		mA
$I_{TRIP(2A)}$	Programmable trip current	ISETx[7:0] = 0x24		500		mA

Note 4 Parts are tested at 25°C and 95°C. Temperature limits established by characterization and are not production tested.
Note 5 Exceeding $t_{TIMEOUT}$ will reset the SMBus state machine, therefore setting SDA and SCL pins to a high impedance state.

Pin Functions

NAME	PIN	IO (Note 7)	DESCRIPTION
VR18	1	P	Internally generated 1.8V power supply for internal circuitry. Decouple to GND with a capacitor.

NAME	PIN	IO (Note 7)	DESCRIPTION
GND	2, 16, 18, 19	P	Ground
V33	3	P	Bias power supply. Decouple to GND with a capacitor.
VDDQ_IN	4-6, 13-15	P	Linear regulator input. Decouple to GND with a capacitor.
VDDQ_OUT	7-12	P	Linear regulator output. Decouple to GND with a capacitor.
ACT	17	I	Activity input. Polarity digitally programmable. Optionally used to indicate system activity. Connect directly to GND if not used. Do not leave floating.
SDA	20	IOD	SMBus data input/output.
SCL	21	IOD	SMBus clock input.
SAx	22-24	I	SMBus address input. This configures the device to one of eight different SMBus addresses.
Pad	25	T	Thermal pad, connect to copper pour for heat dissipation.

Note 7 P = Power, A = Analog, I = Input, O = Output, OD = Open Drain, IOD = Bidirectional Open Drain, T = Thermal, X = Unconnected

1 Ultra-Low Dropout Linear Regulator

A programmable ultra-low dropout linear regulator with a bypass mode is provided to power VDDQ of memory chips. The input to this regulator, VDDQ_IN, is typically provided by the motherboard bulk VDDQ regulator at a nominal voltage. The output voltage programming and bypass features are controlled by On-Demand Power®. With On-Demand Power disabled, the linear regulator is disabled and the bypass switch is closed.

1.1 External Components

The linear regulator requires a minimum of 100µF of low ESR capacitance on the output. Typically this is provided with ceramic capacitors including both bulk capacitance and the distributed bypass capacitors on a memory module.

2 1.8V Linear Regulator

One 1.8V, 15mA linear regulator is provided to power the internal digital logic of the PSG2410 through power pin VR18. An external decoupling capacitor is required between VR18 and GND. This capacitor may be ceramic and should be 1µF.

3 On-Demand Power® Operation

PSG2410 internal registers are programmable via SMBus to control On-Demand Power (ODP) circuitry. Activity is monitored by the programmed current sense and the ACT input. When the ODPEN bit of ODPCON is set, the corresponding output voltage will be managed based on configuration settings and signals gathered from activity sensing inputs. SMBus writes are required to modify the registers for ODP operation. Alternatively, the PSG2410 can be configured to store settings in internal one-time-programmable memory. Contact Packet Digital for details.

3.1 Output Voltage

Once ODP is enabled, output voltage will vary based on system demand, managed by ODP algorithms. Voltages for activity states correspond to the voltage levels set in the ODPVOUTx registers. For high activity (state 0) the bypass switch is engaged, passing through the unmodified VDDQ level. Typical output voltages are defined by the following equation:

$$V_{OUT,typ} = 1.6\text{V} - \frac{ODPVOUTx}{255}$$

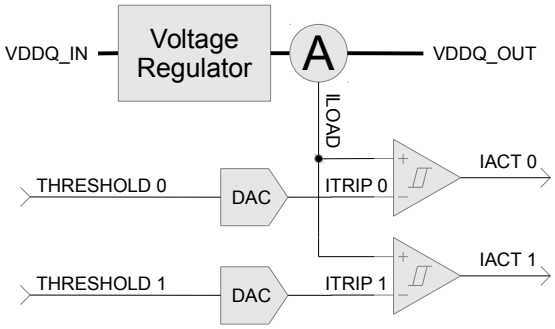
3.2 ACT Input

The ACT pin is a system control input for the ODP algorithm. A logic high signal on this pin indicates a transition to a higher power state. The polarity of this signal can be inverted with the ACTCON register.

3.3 Current Sense

The load current sense circuit detects if the load current is above or below programmable thresholds. There are two thresholds that may be used for the ODP algorithm. The output of the current sensor, I_{LOAD}, is compared to two programmable thresholds through a pair of 8-bit DACs and generates two activity signals that can be selected as activity signals for the ODP algorithm. Typical current thresholds are defined by the following equation:

$$i_{TRIP,typ} = 3.5\ A \cdot \frac{ODPITHx}{255}$$



3.4 ODP Algorithm Activity Inputs

Configuring the input signal to the ODP algorithm is done through the configuration register ODPACT. The PSG2410 has one digital activity input pin and two current sense circuits. The digital input can be used for either ODP activity state. The current sense detectors are independent and are dedicated to their corresponding activity states. If two activity signals are asserted simultaneously, e.g. the digital input is selected for both non-idle states, the higher activity state (0) takes precedence. The following table shows how the algorithm inputs are controlled by these bits:

Input Select 1	Input Select 0	ODP State Activity
0	0	None
0	1	Digital Only
1	0	Current Sense Only
1	1	Digital OR Current Sense

3.5 Timeouts

Transitions to lower activity states are controlled by timeouts. These timeouts are 16-bit values running at the the PSG2410 oscillator speed (4MHz typical). There are separate timeouts for states 0 and 1. The timers begin counting when the activity signal configured for the state is deasserted.

4 Two Wire Interface

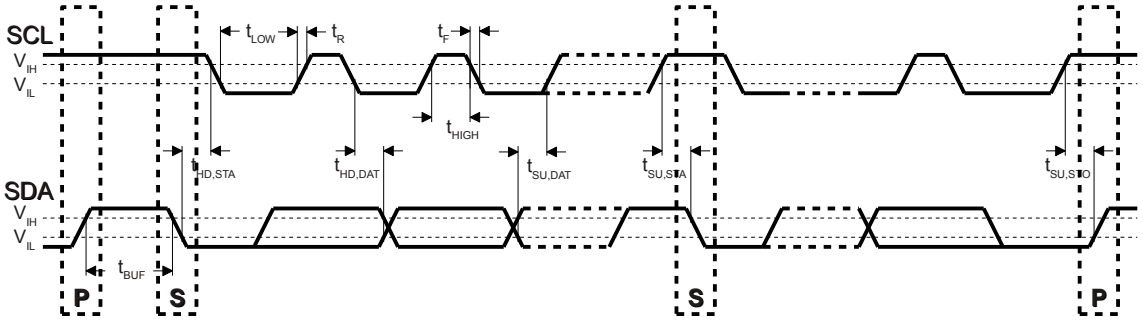
The PSG2410 serial interface is compatible with the SMBus 2.0 specification. SCL is the serial clock input and SDA is the bidirectional serial data. PSG2410 supports 'read byte', 'write byte', and 'block write' as described by the SMBus specification.

4.1 Serial Address

PSG2410 is configured as a slave and has a fixed 7-bit slave address of 0100XXX (0x20 – 0x27), configurable through digital input pins SA0, SA1, and SA2. Tie each SAx pin to GND for logic 0 and V33 for logic 1. The following table outlines SAx pin operation:

SA2	SA1	SA0	Serial Address
0	0	0	0x20
0	0	1	0x21
0	1	0	0x22
0	1	1	0x23
1	0	0	0x24
1	0	1	0x25
1	1	0	0x26
1	1	1	0x27

4.2 Timing Diagram



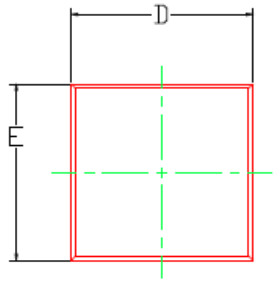
4.3 Address Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	NAME
0x00-0x03	Reserved								RESERVED
0x04	Reserved							Input Polarity	ACTCON
0x05-0x0F	Reserved								RESERVED
0x10	Reserved					OTSTAT 140	OTSTAT 120	OCSTAT	VREGSTAT
0x11	Reserved			VIN Level	ODP_STATE		Reserved	ODP_EN	ODPCON
0x12	ODP State 1 Output Voltage (High Range)								ODPVOUT1_HIGH
0x13	ODP State 2 Output Voltage (High Range)								ODPVOUT2_HIGH
0x14	ODP State 0 Current Threshold (High Range)								ODPITH0_HIGH
0x15	ODP State 1 Current Threshold (High Range)								ODPITH1_HIGH
0x16	ODP Timeout 0 [7:0]								ODPTOUT0_0
0x17	ODP Timeout 0 [15:8]								ODPTOUT0_1
0x18	ODP Timeout 1 [7:0]								ODPTOUT1_0
0x19	ODP Timeout 1 [15:8]								ODPTOUT1_1
0x1A	Reserved				State 1 Input Select		State 0 Input Select		ODPACT (Note 8)
0x1B	Reserved								RESERVED
0x1C	Clock Cycles Per Code to Slew Up to State 0				Codes Per Clock Cycle to Slew Up to State 0				ODPSLEWUP0
0x1D	Clock Cycles Per Code to Slew Up to State 1				Codes Per Clock Cycle to Slew Up to State 1				ODPSLEWUP1
0x1E	Clock Cycles Per Code to Slew Down to State 1				Codes Per Clock Cycle to Slew Down to State 1				ODPSLEWDWN0
0x1F	Clock Cycles Per Code to Slew Down to State 2				Codes Per Clock Cycle to Slew Down to State 2				ODPSLEWDWN1
0x20	VOUT Code to Enter Bypass When Slewing to State 0 (High Range)								ODPSLEWBYPASS
0x21	ODP State 1 Output Voltage (Low Range)								ODPVOUT1_LOW
0x22	ODP State 2 Output Voltage (Low Range)								ODPVOUT2_LOW
0x23	ODP State 0 Current Threshold (Low Range)								ODPITH0_LOW
0x24	ODP State 1 Current Threshold (Low Range)								ODPITH1_LOW
0x25	VOUT Code to Enter Bypass When Slewing to State 0 (Low Range)								ODPSLEWBYPASS_LOW
0x26	Reserved					Level Detect			VIN_DETECT_TH
0x27-0xFF	Reserved								RESERVED

Note 8 Use a read-modify-write operation to preserve the reserved bits when updating this register.

Packaging

The PSG2410 is packaged in a 5mmX5mm 24-pin QFN. All dimensions are in millimeters unless otherwise noted.



DIMENSION (mm)				
SYMBOL	MIN	NOM	MAX	TOL.
A		0.850		+/- 0.1
A3		0.203		
b	0.250	0.300	0.350	
D		5.000		
D2	3.150	3.250	3.350	
E		5.000		
E2	3.150	3.250	3.350	
e		0.650		
L	0.350	0.400	0.450	
θ	0 deg.		14 deg.