Application Note

On-Demand Power® Applications

Setting ODP Registers

Executive Summary

This Application Note discusses how to calculate and set the parameters affecting Packet Digital's patented On-Demand Power®. This note directly references the PSG5220 and other PowerSage® products.

1 Introduction

The output voltages of the PSG5220 are manually configured by writing values to registers internal to the chip. Optimizing output voltage levels and other configuration settings will maximize the power savings On-Demand Power® (ODP) will be able to deliver to your system. This Application Note will allow you to become more comfortable setting the On-Demand Power registers.

2 SMBUS Communication

The PSG5220 On-Demand Power registers are accessed via a two-wire serial interface which is compatible with the SMBUS 2.0 specification. SMBCLK is the serial clock input and SMBDAT is the bidirectional serial data. PSG5220 is configured as a slave on the SMBUS and has a fixed 7-bit slave address of 0x61. PSG5220 supports 'read byte', 'write byte', and 'block write' as described by the SMBUS specification.

The complete register map for PSG5220 can be found in the PSG5220 datasheet.

3 Manual Output Voltage Configuration

When On-Demand Power is disabled, the PSG5220 operates as a static-output voltage regulator. The output voltage can be manually adjusted using the SMBUS serial interface through the registers ODP1VMAN or ODP2VMAN. PSG5220 uses ODP1VMAN and ODP2VMAN for output channels 1 and 2, respectively.

The following formula can be used to calculate the register code for a desired output voltage:

$$Reg_{value} = -85(V_O - 5)$$

Reg_{value} will be a decimal number which will have to be rounded to the nearest whole number and converted to hexadecimal before being written to a register. The output voltage will change immediately when the SMBUS write is complete. A list of common register settings can be found in Table 1. The minimum output voltage for the PSG5220 is 3.0V with a register value of 0xAA.

Table 1: Output Voltage Register Settings

Vout	Reg_{value}(Decimal)	Register Code
5.0V	0	0x00
4.9V	8	0x08
4.8V	17	0x11
4.7V	25	0x19
4.6V	34	0x22
4.5V	42	0x2A
4.4V	51	0x33
4.3V	59	0x3b
4.2V	68	0x44
4.1V	76	0x4C
4.0V	85	0x55

4 On-Demand Power® using nACT

When using the PSG5220 to power a device with an activity signal, the output voltage will scale in reaction to a high or low signal. The “high” and “low” output voltage levels to power a device are reconfigurable in system. Properly tuned voltages will maximize the power savings the PSG5220 will be able to deliver.

Once desired voltages are chosen, the proper codes need to be written to registers 06H and 07H for channel 1 or 25H and 26H for channel 2. When nACT1 is high, V_{O1} will correspond to the value written to register 06H; when nACT1 is low, V_{O1} will correspond to the value written to register 07H. Similar to channel 1, when nACT2 is high, V_{O2} will correspond to the value written to register 25H; when nACT2 is low, V_{O2} will correspond to the value written to register 26H. The values to be written to each register and their corresponding voltages are the same as ODP1VMAN and ODP2VMAN and can be found by using the same procedure as discussed in Section 3 or by referencing Table 1.

5 On-Demand Power® using Current Sense

On-Demand Power can be programmed to dynamically scale based on the load current instead of an activity signal. Though these two methods work very similarly, some extra parameters need to be calculated when using current sensing in place of an activity signal.

5.1 Choosing Rsense

The load current sense circuit in Figure 1 detects if the load current I_L is above or below a programmable threshold I_{TRIP}. A high-side current sense amplifier gains the voltage V_{CS} across a sense resistor R_{SENSE} in response to the load current I_L. The output of the current sense amplifier is compared to a programmable threshold voltage V_{TRIP} that is set using an internal 8-bit DAC. The output of the comparator circuit is high if I_L is greater than I_{TRIP} and low if I_L is less

than I_{TRIP}. The comparator includes internal hysteresis to help reject noise.

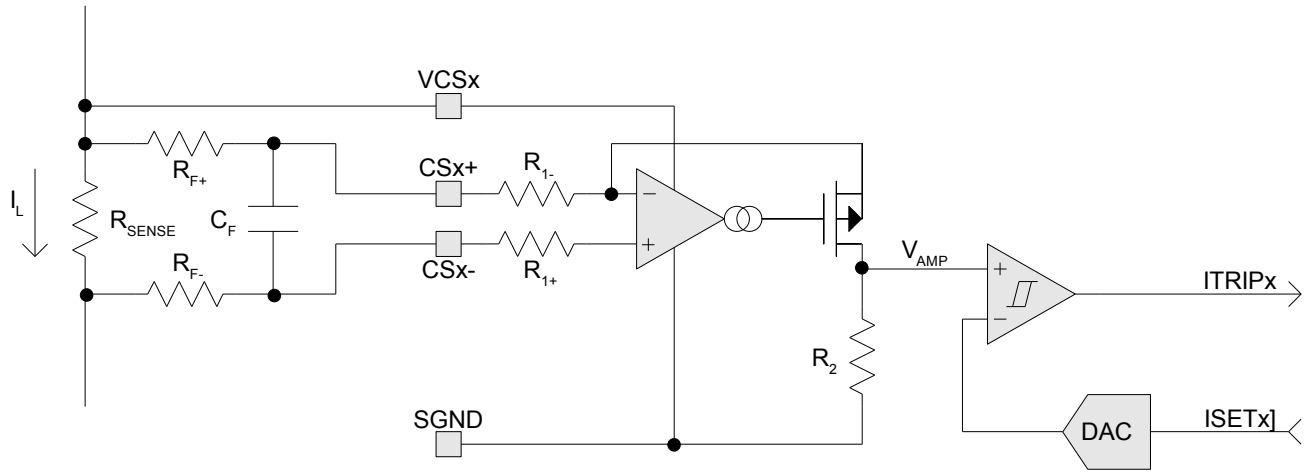

Figure 1: Current Sense Circuitry (One Channel)

The load current sense resistor R_{SENSE} should be selected such that the maximum voltage drop $V_{cs(MAX)}$ across the sense resistor does not exceed the maximum differential input voltage of the current sense amplifier. For a maximum load current of I_{MAX}, the maximum value of R_{SENSE} is:

$$R_{SENSE(MAX)} = \frac{V_{CS(MAX)}}{I_{MAX}}$$

Likewise, the minimum value for R_{SENSE} depends on the minimum load current $I_{TRIP(MIN)}$ that must be detected:

$$R_{SENSE(MIN)} = \frac{V_{CS(MIN)}}{I_{TRIP(MIN)}}$$

It is recommended to choose a sense resister so that $10mV \leq V_{cs} \leq 90mV$.

5.2 Setting Current Threshold

To set the current sense threshold, the voltage across the sense resister, V_{cs} needs to be calculated for the desired I_L trip current. This is the current threshold where V_O will scale from a high state voltage to a low state voltage and also transition from low state to high state. V_{cs} can be found using the following equation:

$$V_{CS} = I_L \times R_{SENSE}$$

Once V_{cs} has been calculated, the correct value for either register 0BH to configure channel 1 or register 2AH to configure channel 2 is found using the following equation:

$$Reg_{value} = ((V_{CS} - 10) \times \frac{91}{40}) + 16$$

Reg_{value} will be a decimal number which will have to be rounded to the nearest whole number and converted to hexadecimal before being written to a register. A list of common register settings can be found in Table 2.

Table 2: Current Sense Voltage Register Settings

Vcs (mV)	Reg_{value}(Decimal)	Register Code
10.000	16	0x10
20.110	39	0x27
30.220	62	0x3E
39.890	84	0x54
50.000	107	0x6B
60.110	130	0x82
70.220	153	0x99
79.890	175	0xAF
90.000	198	0xC6

Just as the voltage levels were set in section 3 when using nACT to trigger voltage scaling, codes also need to be written to tell On-Demand Power which voltage levels to switch between when using current sensing. Once again, the registers to be written are 06H and 07H for channel 1 or 25H and 26H for channel 2. When I_L is above the current sense threshold, V_{O1} will correspond to the value written to register 06H; when I_L is below the current sense threshold, V_{O1} will correspond to the value written to register 07H. Similar to Channel 1, when I_L is above the current sense threshold, V_{O2} will correspond to the value written to register 25H; when I_L is below the current sense threshold, V_{O2} will correspond to the value written to register 26H. The values to be written to each register and their corresponding voltages are the same as ODP1VMAN and ODP2VMAN and can be found by using the same procedure as discussed in Section 3 or by referencing Table 1.

6 Setting Slew Rates and Timeout

Other parameters that affect On-Demand Power voltage scaling are the step up slew rate, step down slew rate, and the OPD timeout. See Figure 2. These are needed whether you use nACT or current sensing to trigger On-Demand Power voltage scaling.

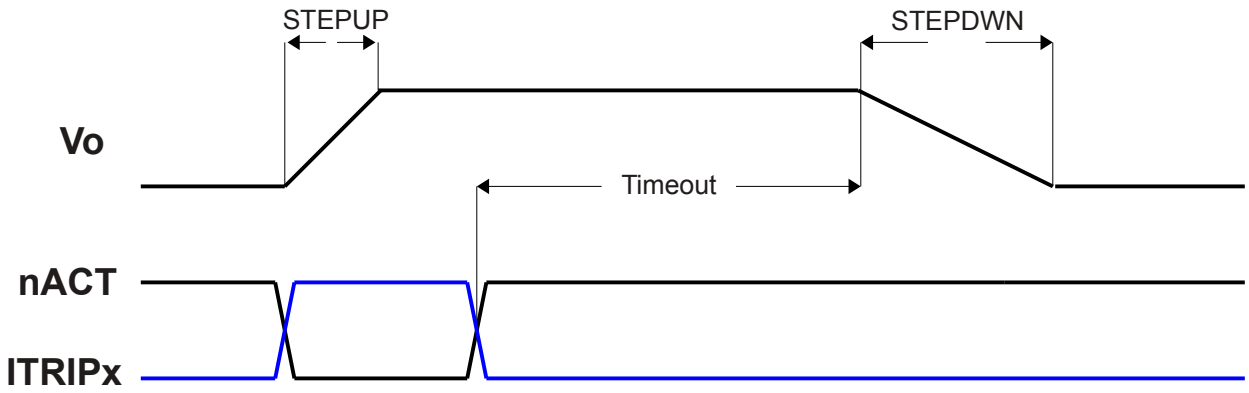

Figure 2: Slew Rates and ODP Timeout

When a trigger from either the nACT signal or current sensing circuitry is detected, there is a soft voltage transition which uses a slew rate to ramp up or ramp down the control byte sent to the DAC which controls V_O. The value from the ODPxSTEPUP registers are used to control the up-slope and the value from the ODPxSTEPDWN registers are used to control the down-slope for voltage transitions. Table 3 shows the corresponding register addresses.

Table 3: Slew Rate Register Settings

Address	Name	Channel
0FH	ODP1STEPUP	1
10H	ODP1STEPDWN	1
2EH	ODP2STEPUP	2
2FH	ODP2STEPDWN	2

If a given step register is set to 00h, then soft transition is disabled for that direction. When a given register does not equal 00h, the register value specifies the number of DAC clock cycles to wait before incrementing/decrementing the control byte sent to the DAC by 01h (approximately 44 mV) resulting in a stair-case like transition from the old value to the new value. Since the internal DAC runs at 500kHz, the following equation is used to calculate time between voltage steps:

$$DAC_{wait} = Reg_{value} \times 2\mu s$$

The PSG5220 also features a timeout which helps to avoid unwanted voltage scaling triggered by state changes occurring very close together. This timeout will hold V_O in the high voltage state, and will only allow V_O to transition to the low voltage state if there are no further triggers during the timeout. The concatenation of ODPxTOUT0_3, ODPxTOUT0_2, ODPxTOUT0_1, and ODPxTOUT0_0 forms the 32-bit register ODPxTOUT0 that specifies the number of DAC clock cycles to wait for the timeout. Table 4 shows the specific registers for channel 1 and channel 2 timeouts.

Table 4: On-Demand Power® Timeout Register Settings

Address	Name	Channel
12H	ODP1TOUT0_0	1
13H	ODP1TOUT0_1	1
14H	ODP1TOUT0_2	1
15H	ODP1TOUT0_3	1
31H	ODP2TOUT0_0	2
32H	ODP2TOUT0_1	2
33H	ODP2TOUT0_2	2
34H	ODP2TOUT0_3	2

Since the internal DAC runs at 500kHz, the following equation would be used to calculate the timeout for channel 1:

$$\text{Timeout} = \text{ODP1TOUT0} \times 2\mu s$$

ODP1TOUT0 will need to be written as a 32 bit hexadecimal number spanning the 4 registers ODPxTOUT0_3, ODPxTOUT0_2, ODPxTOUT0_1, and ODPxTOUT0_0, with register ODPxTOUT0_3 containing the most significant bit.

7 Enabling On-Demand Power®

Once all On-Demand Power registers have been written, On-Demand Power can be enabled. For the PSG5220, the following registers are responsible for enabling and disabling ODP. The code to be written will depend on whether nACT or current sensing is used to trigger ODP voltage scaling. See Table 5 and Table 6.

Table 5: Enable/Disable On-Demand Power® for Channel 1

Function	Address	Data
Enable	0x03	
	nACT	0x09
	Current Sense	0x0D
Disable	0x03	0x08

Table 6: Enable/Disable On-Demand Power® for Channel 2

Function	Address	Data
Enable	0x22	
	nACT	0x09
	Current Sense	0x0D
Disable	0x22	0x08

8 Design Example

Table 7 is an example of register settings which were supplied to Intel specifically for their Elk Hill 2 platform.

Table 7: Intel's Elk Hill 2 Register Settings

Register	0x10	0x12	0x13	0x16	0x17	0x1F	0x06	0x07	0x08	0x09	0x0B	0x0C
Code	0x1F	0x50	0xC3	0x50	0xC3	0x82	0x29	0x3A	0x3A	0x3A	0x24	0x24